REMARKS

This response is accompanied by a Petition for Extension of Time for one month, up to and including November 12, 2007, and the required fee. Please charge the required extension of time fee or credit any overpayment to Deposit Account No. 50-1698.

In the Office Action mailed July 11, 2007 claims 1-11 were rejected under 35 U.S.C. § 102(b) as being allegedly anticipated by U.S. Patent No. 6,115,278 to Deneroff et al. (Deneroff).

On October 22, 2007, Applicant's representative conducted a telephonic interview with Examiner Dinh. Applicant thanks the Examiner for the courtesy of allowing this interview. During the interview, the rejection of pending claims over Deneroff reference was discussed and an agreement was reached that Deneroff fails to anticipate claims 1-11 of the present application. Following is the recitation of the arguments advanced by the Applicant's representative during the interview with Examiner Dinh.

According to the M.P.E.P., a claim is anticipated under 35 U.S.C. § 102(a), (b) and (e) only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.[1] Applicant submits that Deneroff fails to anticipate claims 1-11 of the present application because Deneroff does not disclose, teach or even suggest a memory module comprising, *inter alia*, "a printed circuit board having a plurality of connector pins, [and] a plurality of different types of memory devices mounted on said printed circuit board...," as recited in independent claims 1 and 8, as well as a method for creating such a memory module as recited in independent claim 10.

In contrast, Deneroff discloses a memory system that includes a plurality of memory modules, such as Dual Inline Memory Module (DIMM). *See*, e.g., col. 2, ll. 40-47; and col. 3, ll.

[1] Manual of Patent Examining Procedure (MPEP) § 2131.

5-8. Each memory module includes a plurality of memory devices, such as Dynamic Random-Access Memory (DRAM) devices. *See*, e.g., col. 5, ll. 43-49. The memory devices may be placed on both sides of the memory module. See, e.g., col. 7, ll. 40-64; and Figs. 3 and 4. More specifically, Deneroff discloses that in one embodiment all memory devices on both sides of a memory module may be 8 megabit DDR SDRAMs, and, in alternative embodiment, all memory devices may be 16 megabit DDR SDRAMs. *See*, col. 7, ll. 58-64. In other words, in each alternative embodiment, a memory module includes memory devices of the same type.

As pointed by the Applicant's representative during interview with Examiner Dinh, the memory system disclosed by Deneroff differs from the memory configuration claimed in the present application at least in that that the claimed memory module contains a plurality of different types of memory devices, such as DDR SDRAM, FCRAM, RLDRAM and the like. *See*, e.g., claims, 1, 2, 8 and 10. While Deneroff discloses a memory system in which each memory module contains only one type of memory devices, such as 8 or 16 megabit DDR SDRAM. Moreover, Deneroff does not disclose, teach or even suggest that a single memory module may contain different types of memory devices, as recited in claims 1, 8, 10.

Accordingly, independent claims 1, 8 and 10 are patentable over Deneroff. As to dependent claims 2-7, 9 and 11, the argument set forth above is equally applicable here. The base claims being patentable, the dependent claims must also be patentable.

In view of the above, Applicant submits that the present application is in condition for allowance. A favorable disposition to the effect is respectfully requested.

Respectfully submitted,

Dated: November 12, 2007

Suvashis Bhattacharya
Reg. No.46,554

Thelen Reid Brown Raysman & Steiner LLP
P.O. Box 640640
San Jose, CA 95164-0640
Tel. (408) 292-5800
Fax. (408) 287-8040